In the Claims:

Claim 1 (currently amended): A high-k dielectric stack situated between an upper electrode and a lower electrode of a MIM capacitor, said high-k dielectric stack comprising:

a first high-k dielectric layer, said first high-k dielectric layer having a first dielectric constant;

an intermediate dielectric layer situated on said first high-k dielectric layer, said intermediate dielectric layer having a second dielectric constant;

a second high-k dielectric layer situated on said intermediate dielectric layer, said second high-k dielectric layer having a third dielectric constant;

wherein said second dielectric constant is not greater than said first dielectric constant and said third dielectric constant;

wherein said intermediate dielectric layer forms an interface with each of said first high-k dielectric layer and said second high-k dielectric layer to impede electron flow between said upper and lower electrodes of said MIM capacitor.

Claim 2 (original): The high-k dielectric stack of claim 1 further comprising first and second cladding layers, said first cladding layer being situated underneath said first high-k dielectric layer and said second cladding layer being situated on said second high-k dielectric layer.

Claim 3 (original): The high-k dielectric stack of claim 1 wherein said second dielectric constant is less than said first dielectric constant and said third dielectric constant.

Claim 4 (original): The high-k dielectric stack of claim 1 wherein said intermediate dielectric layer comprises Al_2O_3.

Claim 5 (original): The high-k dielectric stack of claim 1 wherein said intermediate dielectric layer has a thickness between approximately 5.0 Angstroms and approximately 70.0 Angstroms.

Claim 6 (original): The high-k dielectric stack of claim 2 wherein said first cladding layer is situated on said lower electrode and said upper electrode is situated on said second cladding layer.

Claim 7 (original): The high-k dielectric stack of claim 6 wherein said lower electrode comprises Ti/TiN and wherein said upper electrode comprises TiN.

Claim 8 (original): The high-k dielectric stack of claim 1 wherein said first and second high-k dielectric layers are selected from the group consisting of HfO_2 and Ta_2O_5.

Claim 9 (currently amended): A method for fabricating a MIM capacitor in a semiconductor die, said method comprising steps of:

forming a lower electrode of said MIM capacitor;

forming a first high-k dielectric layer over said lower electrode, said first high-k dielectric layer having a first dielectric constant;

forming an intermediate dielectric layer on said first high-k dielectric layer, said intermediate dielectric layer having a second dielectric constant;

forming a second high-k dielectric layer on said intermediate layer, said second high-k dielectric layer having a third dielectric constant;

forming an upper electrode of said MIM capacitor over said second high-k dielectric layer;

wherein said second dielectric constant is not greater than said first dielectric constant and said third dielectric constant;

wherein said intermediate dielectric layer forms an interface with each of said first high-k dielectric layer and said second high-k dielectric layer to impede electron flow between said upper and lower electrodes of said MIM capacitor.

Claim 10 (original): The method of claim 9 further comprising the steps of:

forming a first cladding layer on said lower electrode before said step of forming said first high-k dielectric layer;

forming a second cladding layer on said second high-k dielectric layer after said step of forming said second high-k dielectric layer.

Claim 11 (original): The method of claim 9 wherein said second dielectric constant is less than said first dielectric constant and said third dielectric constant.

Claim 12 (original): The method of claim 9 wherein said intermediate dielectric layer comprises Al_2O_3.

Claim 13 (original): The method of claim 9 wherein said intermediate dielectric layer has a thickness between approximately 5.0 Angstroms and approximately 70.0 Angstroms.

Claim 14 (original): The method of claim 9 wherein said lower electrode comprises Ti/TiN and wherein said upper electrode comprises TiN.

Claim 15 (original): The method of claim 9 wherein said first and second high-k dielectric layers are selected from the group consisting of HfO_2 and Ta_2O_5.

Claim 16 (currently amended): A MIM capacitor situated in a semiconductor die, said MIM capacitor comprising:

a lower electrode;

a first cladding layer situated on said lower electrode;

a first high-k dielectric layer situated on said first cladding layer, said first high-k dielectric layer having a first dielectric constant;

an intermediate dielectric layer situated on said first high-k dielectric layer, said intermediate dielectric layer having a second dielectric constant;

a second high-k dielectric layer situated on said intermediate dielectric layer, said second high-k dielectric layer having a third dielectric constant;

a second cladding layer situated on said second high-k dielectric layer;

an upper electrode situated on said second cladding layer;

wherein said intermediate dielectric layer forms an interface with each of said first high-k dielectric layer and said second high-k dielectric layer to impede electron flow between said upper and lower electrodes of said MIM capacitor.

Claim 17 (original): MIM capacitor of claim 16 wherein said second dielectric constant is less than said first dielectric constant and said third dielectric constant.

Claim 18 (original): The MIM capacitor of claim 16 wherein said intermediate dielectric layer comprises Al_2O_3.

Claim 19 (original): The MIM capacitor of claim 16 wherein said intermediate dielectric layer has a thickness between approximately 5.0 Angstroms and approximately 70.0 Angstroms.

Claim 20 (original): The MIM capacitor of claim 16 wherein said lower electrode comprises Ti/TiN and wherein said upper electrode comprises TiN.